WHAT IS CLAIMED IS:

1. An integrated circuit having a plurality of active components including junctions formed in a monocrystalline substrate doped locally, and at least one passive component situated above the active components, said integrated circuit comprising:

a first insulating layer separating the active components and a base of the passive component; and

a metal terminal for electrically connecting the passive component with at least one of the active components, the metal terminal being formed in the thickness of the first insulating layer and having a contact surface that projects from the limits of a junction of the one active component.

2. The integrated circuit according to claim 1, wherein the passive component is a capacitor.

3. The integrated circuit according to claim 1, wherein the passive component is an inductor.

4. The integrated circuit according to claim 1,
wherein the thickness of the first insulating layer is greater than 0.3 micrometers,
the top surface of the first insulating layer is plane, and
the metal terminal is made principally of tungsten.

5. The integrated circuit according to claim 1, further comprising a second insulating layer above the first insulating layer, the passive component being set into a cavity formed throughout the thickness of the second insulating layer.

6. The integrated circuit according to claim 5, wherein the thickness of the second insulating layer is greater than 2 micrometers.

7. An integrated circuit including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:

a first metal terminal passing completely through the thickness of the first insulating layer, the first metal terminal constituting a first stage of contact between an active area of the integrated circuit and a first level of interconnection;

a second metal terminal passing completely through the thickness of the first insulating layer, the second metal terminal vertically connecting an active area of the integrated circuit to a passive component resting on the first insulating layer; and

a third metal terminal passing completely through the thickness of the first insulating layer, the third metal terminal horizontally connecting two separate active areas of the integrated circuit.

8. The integrated circuit according to claim 7, wherein the second metal terminal has a contact surface projecting from the limits of a junction of an active component.

9. The integrated circuit according to claim 7, wherein the passive components include capacitors.

10. The integrated circuit according to claim 7, wherein the passive components include inductors.

11. The integrated circuit according to claim 7,

wherein the thickness of the first insulating layer is greater than 0.3 micrometers,

the top surface of the first insulating layer is plane, and

the first, second, and third metal terminals are made principally of tungsten.

12. The integrated circuit according to claim 7, further comprising a second insulating layer above the first insulating layer, the passive component resting on the first insulating layer being set into a cavity formed throughout the thickness of the second insulating layer.

13. The integrated circuit according to claim 12, wherein the thickness of the second insulating layer is greater than 2 micrometers.

14. An integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

15. The integrated circuit according to claim 14, wherein the second metal terminal has a contact surface projecting from the limits of a junction of the active area.

16. The integrated circuit according to claim 14, further comprising:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal,

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

17. The integrated circuit according to claim 16, further comprising:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the top surface of the first metal terminal.

18. The integrated circuit according to claim 14, wherein the first, second, and third metal terminals are made principally of tungsten.

19. An information processing system including at least one integrated circuit, the integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit.

20. The information processing system according to claim 19, wherein the second metal terminal has a contact surface projecting from the limits of a junction of the active area.

21. The information processing system according to claim 19, wherein the integrated circuit further comprises:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal,

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

22. The information processing system according to claim 21, wherein the integrated circuit further comprises:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the top surface of the first metal terminal.

23. The information processing system according to claim 19, wherein the first, second, and third metal terminals are made principally of tungsten.

24. A method of fabricating an integrated circuit that includes a plurality of MOS transistors and an onboard memory plane of DRAM cells in a matrix, each of the cells consisting of a control transistor and a storage capacitor, said method comprising the steps of:

forming transistors in a silicon substrate;

depositing a first insulating layer on top of the transistors;

polishing to produce a plane surface on the first insulating layer;

forming cavities through the first insulating layer;

filling the cavities with metal terminals such that a bottom part of a first metal terminal is in electrical contact with at least one component of the underlying integrated circuit, a bottom part of a second metal terminal is in electrical contact with a junction of one of the control transistors, and a bottom part of a third metal terminal is in electrical contact with components of the integrated circuit to be interconnected; and

forming a capacitor above the second metal terminal such that a bottom electrode of the capacitor is in electrical contact with a top part of the second metal terminal.

25. The method according to claim 24, wherein the step of forming a capacitor includes the sub-steps of:

after forming the metal terminals, depositing a second insulating layer that is more than 2 micrometers thick on top of the first insulating layer and the top surface of the second metal terminal;

forming a cavity through the second insulating layer that reaches the top surface of the second metal terminal; and

growing electrodes of the capacitor on the bottom of the cavity and on the flanks of the cavity.

26. The method according to claim 24, wherein the first, second, and third metal terminals are made principally of tungsten.

27. A machine-readable medium encoded with a program for fabricating an integrated circuit that includes a plurality of MOS transistors and an onboard memory plane of DRAM cells in a matrix, each of the cells consisting of a control transistor and a storage capacitor, said program containing instructions for performing the steps of:

forming transistors in a silicon substrate;

depositing a first insulating layer on top of the transistors;

polishing to produce a plane surface on the first insulating layer;

forming cavities through the first insulating layer;

filling the cavities with metal terminals such that a bottom part of a first metal terminal is in electrical contact with at least one component of the underlying integrated circuit, a bottom part of a second metal terminal is in electrical contact with a junction of one of the control transistors, and a bottom part of a third metal terminal is in electrical contact with components of the integrated circuit to be interconnected; and

forming a capacitor above the second metal terminal such that a bottom electrode of the capacitor is in electrical contact with a top part of the second metal terminal.

28. The machine-readable medium according to claim 27, wherein the step of forming a capacitor includes the sub-steps of:

after forming the metal terminals, depositing a second insulating layer that is more than 2 micrometers thick on top of the first insulating layer and the top surface of the second metal terminal;

forming a cavity through the second insulating layer that reaches the top surface of the second metal terminal; and

growing electrodes of the capacitor on the bottom of the cavity and on the flanks of the cavity.

29. The machine-readable medium according to claim 27, wherein the first, second, and third metal terminals are made principally of tungsten.